

Claims

1. A capacitor device, characterized by including:
a plurality of electric double-layer capacitors which are connected in series; and
a balance resistor portion in which m (which is an integer of two or above) resistors having an equivalent resistance are connected in parallel,
the balance resistor portion being connected in parallel to each electric double-layer capacitor.
2. The capacitor device according to claim 1, characterized in that the resistance of the balance resistor portion is equal to, or less than, one-fourth the resistance of each resistor which forms the balance resistor portion.
3. The capacitor device according to claim 1, characterized in that the resistance of the balance resistor portion is equal to, or more than, one-sixth, and the resistance of each resistor which forms the balance resistor portion.
4. The capacitor device according to claim 1, characterized in that the resistance of the balance resistor portion is equal to, or more than, one-sixth the resistance of each resistor which forms the balance resistor portion and is equal to, or less than, one-fourth this resistance.

5. The capacitor device according to claim 1, characterized in that the resistance of the balance resistor portion is 100 Ω or above and 500 Ω or below.

6. The capacitor device according to claim 1, characterized in that the number of electric double-layer capacitors connected in series is set so that a bias voltage given to each electric double-layer capacitor is lower than the rated voltage of the electric double-layer capacitor.

7. The capacitor device according to claim 1, characterized in that one or a plurality of electric double-layer capacitors are further connected in parallel to the balance resistor portion.

8. A wiring pattern in which a plurality of electric double-layer capacitors are connected in parallel, characterized in that:

the wiring pattern includes three or more wiring patterns disposed at a predetermined interval;

a plurality of electric double-layer capacitors are connected in parallel between adjacent wiring patterns; and

between two adjacent electric double-layer capacitors which are connected between the wiring patterns, a plurality of resistors having an equivalent resistance are connected

in parallel to the electric double-layer capacitors.

9. The wiring pattern according to claim 8, characterized in that the resistors are connected from one wiring surface of the wiring pattern, and the electric double-layer capacitors are connected from the other wiring surface of the wiring pattern.